BUS SYSTEM AND BUS INTERFACE FOR CONNECTION TO A BUS

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The invention relates to a bus system comprising a first station (202) and a second station (203), (204), coupled by a bus for transferring messages, said bus being designed t o operate in accordance with a protocol in which said first station (202) periodic ally sends messages in a predetermined order to the second station (203), (204), wherein- said first station (202) comprises an interruptible processor (206), a memory element (208) comprising a buff er (501, 502), and a bus int erface (207),- wherein said int erruptible processor (206) can be operated so as t o generate a plurality of series of message properties; - wherein said proc essor (206) can further be operated so as to issue a first series of message properties from among said pluralit y of series of message proper ties to said buffer (501, 503), and upon receipt of an interrupt signal from said bus interface issues a second series of message properties from among said plurality of series of message properties; - wherein said buf fer (501, 502) has a storage capacity, which is adjustable by the processor (206) and which is matched to store said first series of said message properties and said sec ond series of said message properties; and- wherein said bus interface (207) can be operated so as to retrieve said first series of mess age properties from said buff er, to generate a first series of said m essages from said properties, to send said first series of said messages to said second station (203, 204), and to send said interrupt signal to said processor (206).

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